REMARKS

Claim Status

Claims 1-20 remain for consideration. All claims are thought to be allowable over the cited art.

Claims 6-12 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten.

No amendments are made to the claims, because all claims are thought to be allowable over the cited art.

Rejections Under 35 USC §103(a)

The Office Action fails to establish that claims 1-5, 13-18 and 20 are unpatentable under 35 USC §103(a) over "Agrawal" (US patent 6,216,257 to Agrawal et al.) in view of "Williams" (US patent 6,631,508 to Williams). The rejection is respectfully traversed because Williams is disqualified as prior art under 35 USC §103(c). Furthermore, even if Williams is qualifying prior art, the Office Action does not show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Agrawal with teachings of Williams, and fails to show that the combination could be made with a reasonable likelihood of success.

Williams does not qualify as prior art under 35 USC §103(c). The present application was filed on January 8, 2001 and before publication of Williams, and the present application and Williams were, at the time the invention of the present application was made, owned by or subject to assignment to Xilinx, Inc. Therefore, the rejection of claims 1-5, 13-18, and 20 is moot and should be withdrawn.

Even if Williams qualifies as prior art, the Office Action does not establish that all the limitations are suggested by the Agrawal-Williams combination. For example, claims 1 and 20 include limitations of and related to generating events in response to signal values in the configuration bitstream, each event including an object identifier, an input signal identifier, and an input signal state.

Williams generally describes approaches for placing a circuit design, not methods for simulating. Thus, it is not apparent how the cited teachings of Williams

could be reasonably construed to suggest the claimed generating and processing of events. For example, Williams' column 9 shows example VHDL placement directives, and column 10 describes specific placement directive commands used on placing parts of the design. Furthermore, the cited col. 10, ll. 33-49 contain no apparent suggestion of generating events of any sort, nor any apparent suggestion of generating those events in response to signal values in the configuration bitstream. The further limitations that relate to processing of the events are likewise not suggested. An explanation is requested if the rejection is maintained.

The alleged motivation for combining Williams with Agrawal is improper. The alleged motivation states that "it would have been obvious ... to modify mapping VHDL constructs to the fine and/or coarse grain resources of the targeted FPGA device/family as taught in Agrawal with the steps as disclosed in Williams since the mapping step involves mapping the netlist to particular configurable resources of the device as taught in Williams.". The alleged motivation is improper because it fails to provide any evidence that Agrawal's approach for mapping is in any way deficient, fails to provide any evidence to indicate what improvement Williams' teachings might offer, and even fails to provide evidence of how teachings of Agrawal's might be modified to accommodate Williams' approach. It is not apparent how Agrawal's method could be modified with teachings of Williams.

Furthermore, the further alleged reasons provided in the *Response to Arguments* in the recent Office Action provide no evidence of a motivation to combine any of the teachings. The further alleged reasons are that "both Agrawal and Williams teach methods for placing an FPGA design and simulating this design at various points in the design process." Simply because two references are in similar art areas is not itself evidence of a motivation to combine teachings. Therefore, the alleged motivation is improper.

The rejection of claims 1 and 20 over the Agrawal-Williams combination should be withdrawn because Williams is disqualified as prior art under 35 USC §103(c), and the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

As to claims 2 and 15, the further limitations include constructing lookup table objects corresponding to FPGA lookup tables, wherein each lookup table object includes a plurality of input signal attributes and an ordered set of bit values, and each bit value is addressable by values of the input signal attributes. The Office Action fails to show that Agrawal suggests these limitations. The cited col. 8, ll. 40-44 simply states that a Boolean function may be implemented with a lookup table (LUT). In no apparent way does this suggest constructing lookup table objects corresponding to FPGA lookup tables. In Agrawal, the LUTs exist in the FPGA, and there is no apparent need to construct objects that correspond to the LUTs. Thus, the limitation of claims 2 and 15 are not shown to be suggested by Agrawal.

Claims 3 and 16 include further limitations of each event further including a routing delay value. The cited col. 9, ll. 52-58 and Table 1 neither teach nor suggest these limitations. Neither the text nor the Table make any apparent reference to an event or any association of a routing delay value with the event. Therefore, the Office Action fails to show that Agrawal suggests the limitations of claims 3 and 16.

Claims 4 and 17 include further limitations of and related to adding each event to a last-in-first-out (LIFO) queue, and getting each event from the LIFO queue prior to processing the event. The cited col. 3, ll. 33-36 teaches that embedded run-time memory in an FPGA may be used to queue data words. There is no apparent reasonable reading of Agrawal's teachings that suggest adding events generated in response to a configuration bitstream to or removing the events from a LIFO queue. Thus, the Office Action fails to show that the limitations of claims 4 and 17 are suggested by Agrawal.

Claims 5 and 18 include further limitations of and related to maintaining a synchronous event LIFO queue for synchronous events and an asynchronous event LIFO queue for asynchronous events. The cited teaching at col. 8, l. 66 – col. 9, l. 10 clearly does not suggest these limitations. The cited text states:

> The VHDL descriptions 20 may further include timing constructs 24 that define whether various signals are synchronous or asynchronous with respect to various clocks. Example could include clock-synchronized registers and tri-stated buses. The timing constructs 24 may further set forth minimum and maximum timing constraints for various signals.

> The VHDL descriptions 20 may additionally include input/output constructs 25 that define the pinouts of the to-be-implemented device and define whether each pin is synchronous or asynchronous and unidirectional or bidirectional (tri-stateable).

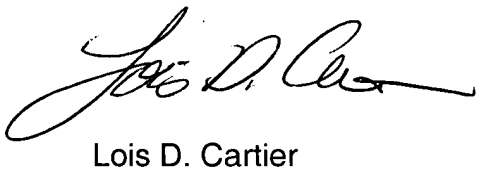
As is clearly evident from the text, there is no suggestion of a synchronous LIFO queue for synchronous events nor is there a suggestion of an asynchronous LIFO queue for asynchronous events. The text describes VHDL definitions of synchronous and asynchronous signals, not events or any queues maintained for the events. Thus, the limitations of claims 5 and 18 are not shown to be suggested by Agrawal.

Claims 13 and 14 depend from claim 1 and are patentable over the Agrawal-Williams combination for at least the reasons set forth above.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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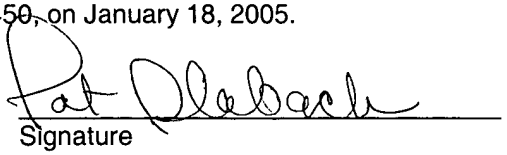
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